Usage Report for Fiscal Year 2023

Project Title:

Benchmarking CIM algorithms for solving combinatorial optimization problems

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1. Background and purpose of the project, relationship of the project with other projects

We are developing machines called Ising machines that can solve combinatorial optimization problems using a Field Programmable Gate Array (FPGA). In principle, such machines can solve NP-hard problems faster than the current state of the art. Thus, the goal of this project is to use Hokusai for: 1) Tuning the parameters to optimize the solver capability; 2) Evaluate the solver using different problems; 3) Compare the FPGA results with the CPU results and the state-of-the-art.

2. Specific usage status of the system and calculation method

Two algorithms based on the Ising model are being evaluated: spiking Chaotic Amplitude Control (sCAC) developed with our collaborators, and discrete Simulation Bifurcation Machine (dSBM) developed by Toshiba. Both algorithms are using the same types of problem, ranging from problem size N=100 to N=16000, and generate an optimal solution, a success probability, and the time required to find the optimal solution.

3. Result

Initially, our research demonstrated the superior performance of our developed algorithm and FPGA-based hardware in solving combinatorial optimization problems compared to existing state-of-the-art across various graph types. However, a comparative analysis between the results obtained from our FPGA implementation and Hokusai has revealed certain discrepancies. To address these discrepancies and further enhance the efficiency of our algorithm, improvements have been made. Modifications and optimizations were applied to our algorithmic approach, focusing on refining its solving capability and computation speed. These enhancements aimed to reconcile the disparities observed in the results obtained from our FPGA implementation and those generated by the Hokusai supercomputer. Through these improvements, our goal was to close the performance gaps observed between our FPGA-based solution and the Hokusai supercomputer. The revised algorithm, with its enhanced solving capability and optimized computation speed, presents a more competitive and robust approach in tackling combinatorial optimization problems.

4. Conclusion

In conclusion, the advancements made in refining our algorithm and enhancing the computational performance of our FPGA-based solution represent a significant step forward in addressing the disparities observed in comparison to the results obtained from the Hokusai supercomputer. The modifications and optimizations implemented have improved the solving capabilities and computational efficiency of our approach in tackling combinatorial optimization problems across various graph types. However, while

our revised algorithm demonstrates promising advancements, further investigation is warranted to thoroughly evaluate and validate its improved performance. This entails conducting rigorous testing and benchmarking to comprehensively assess its efficacy, scalability, and robustness across a diverse set of combinatorial optimization problem instances. Moreover, it is imperative to explore and benchmark against other competitive algorithms. Particularly, a comprehensive evaluation of the dSBM algorithm developed by Toshiba, should be undertaken. A comparative analysis against such state-of-the-art algorithms will provide valuable insights into the strengths, weaknesses, and potential areas for further enhancement of our improved version.

５． Schedule and prospect for the future

In the schedule of our future work on the project, our immediate focus involves comprehensive testing and validation of the enhanced algorithm, conducting extensive benchmarking against competitive solutions like Toshiba's dSBM, and publishing the findings. In the future, the plan involves exploring avenues for scalability, adaptability to diverse problem domains, and potential hardware optimizations to harness the full capabilities of FPGA-based computing.

６． If no job was executed, specify the reason.

Fiscal Year 2023 List of Publications Resulting from the Use of the supercomputer